

IN THE CLAIMS

1. (Currently amended) A processor comprising:

first classification circuitry configurable to determine for a given packet ~~received by the processor~~ whether the packet has one or more errors;

the first classification circuitry storing the given packet in both first memory circuitry and second memory circuitry, wherein the given packet is stored in the first memory circuitry with an indication of the error determination made by the first classification circuitry;

scheduling circuitry coupled to the first ~~classification circuitry~~ memory circuitry and adapted to receive therefrom the given packet and an ~~the~~ indication of the error determination made by the first classification circuitry; ~~and~~

second classification circuitry coupled to the scheduling circuitry, the second classification circuitry receiving the given packet from the scheduling circuitry if the error determination indication meets one or more specified criteria; and

logic circuitry having inputs coupled to respective outputs of the scheduling circuitry and the second classification circuitry, the logic circuitry controlling the dispatch of the given packet from the second memory circuitry responsive to signals from the scheduling circuitry and the second classification circuitry;

~~the scheduling circuitry being configurable based on the indication of the error determination to control the performance of at least one of: (i) dropping of the given packet, and (ii) directing the given packet to the second classification circuitry~~

wherein if the error determination indication does not meet the one or more specified criteria, the given packet is dropped from the first memory circuitry and the second memory circuitry responsive to one or more signals from the scheduling circuitry.

2. (Original) The processor of claim 1 wherein the scheduling circuitry is configurable based on the indication of the error determination to control the dropping of the packet if the packet has one or more errors.

3. (Original) The processor of claim 1 wherein the scheduling circuitry is configurable based on the indication of the error determination to direct the given packet to the second classification circuitry if the packet does not have one or more errors, the second classification circuitry being configurable to perform at least one classification operation for the given packet if the packet is supplied thereto by the scheduling circuitry.

4. (Original) The processor of claim 1 wherein the processor is configured to provide an interface for communication of the packet between a network and a switch fabric.

5. (Original) The processor of claim 1 wherein particular classification operations performed by at least one of the first and second classification circuitry are programmable via software deliverable to the processor via an associated host device.

6. (Original) The processor of claim 1 wherein the first classification circuitry comprises a preclassifier configured to perform at least a portion of at least one of a reassembly operation, a parity check and a priority determination for the given packet.

7. (Original) The processor of claim 1 wherein the second classification circuitry comprises at least one classifier engine configured to generate a transmit command specifying a destination identifier for the given packet as supplied thereto by the scheduling circuitry if the packet does not have one or more errors.

8. (Currently amended) The processor of claim 1 further comprising the first memory circuitry and the second memory circuitry, at least a portion of the packet being storable substantially simultaneously in the first and second memory circuitry.

9. (Currently amended) The processor of claim 8 1 wherein the first memory circuitry and the second memory circuitry comprise different portions of a single memory internal to the processor.

10. (Currently amended) The processor of claim 8 1 wherein the first memory circuitry and the second memory circuitry comprise different memories, at least one of which is internal to the processor.

11. (Currently amended) The processor of claim 8 1 wherein the first memory circuitry comprises a queuing and dispatch buffer memory of the processor.

12. (Currently amended) The processor of claim 8 1 wherein the second memory circuitry comprises a packet buffer memory of the processor.

13. (Currently amended) The processor of claim 1 ~~further comprising~~ wherein the logic circuitry comprises queuing and dispatch logic circuitry coupled to at least the scheduling circuitry and the second classifier circuitry, the queuing and dispatch logic receiving from the scheduling circuitry a flush command directing that the packet be dropped if the packet has one or more errors, and receiving from the second classification circuitry a transmit command directing that the packet be transmitted to a particular destination if the packet does not have one or more errors.

14. (Currently amended) The processor of claim 1 wherein the indication of the error determination made by the first classification circuitry comprises an error flag, the error flag being set in the first memory circuitry ~~of the processor~~ and supplied therefrom to the scheduling circuitry.

15. (Currently amended) The processor of claim 1 wherein one or more parameters associated with at least one operation of at least one of the first classification circuitry, the scheduling circuitry

and the second classification circuitry ~~is~~ are determined in accordance with one or more instructions provided to the processor under control of a host device operatively coupled to the processor.

16. (Original) The processor of claim 1 wherein the processor comprises a network processor.

17. (Original) The processor of claim 1 wherein the processor is configured as an integrated circuit.

18. (Currently amended) A method for use in a processor comprising first and second classification circuitry coupled to scheduling circuitry, the method comprising the steps of:

determining in the first classification circuitry, for a given packet ~~received by the processor~~, whether the packet has one or more errors, the first classification circuitry generating an indication of the error determination, the error determination indication being made accessible to the scheduling circuitry; and

~~based on the error determination indication, performing at least one of: (i) dropping the packet, and (ii) directing the packet from the scheduling circuitry to the second classification circuitry~~

storing the given packet in both first memory circuitry and second memory circuitry, wherein the given packet is stored in the first memory circuitry with an indication of the error determination made by the first classification circuitry;

receiving, in the scheduling circuitry from the first memory circuitry, the given packet and the indication of the error determination made by the first classification circuitry;

receiving, in the second classification circuitry from the scheduling circuitry, the given packet if the error determination indication meets one or more specified criteria; and

controlling the dispatch of the given packet from the second memory circuitry responsive to signals from the scheduling circuitry and the second classification circuitry;

wherein if the error determination indication does not meet the one or more specified criteria, the given packet is dropped from the first memory circuitry and the second memory circuitry responsive to one or more signals from the scheduling circuitry.

19. (Original) The method of claim 18 further including the step of performing in the second classification circuitry at least one classification operation for the given packet if the packet is supplied thereto by the scheduling circuitry.

20. (New) An integrated circuit comprising:

first classification circuitry configurable to determine for a given packet whether the packet has one or more errors;

the first classification circuitry storing the given packet in both first memory circuitry and second memory circuitry, wherein the given packet is stored in the first memory circuitry with an indication of the error determination made by the first classification circuitry;

scheduling circuitry coupled to the first memory circuitry and adapted to receive therefrom the given packet and the indication of the error determination made by the first classification circuitry;

second classification circuitry coupled to the scheduling circuitry, the second classification circuitry receiving the given packet from the scheduling circuitry only if the error determination indication meets one or more specified criteria; and

logic circuitry having inputs coupled to respective outputs of the scheduling circuitry and the second classification circuitry, the logic circuitry controlling the dispatch of the given packet from the second memory circuitry responsive to signals from the scheduling circuitry and the second classification circuitry;

wherein if the error determination indication does not meet the one or more specified criteria, the scheduling circuitry (i) controls the first memory circuitry such that the given packet is flushed from the first memory circuitry, and (ii) directs the logic circuitry to flush the given packet from the second memory circuitry.